CALIFORNIA STATE UNIVERSITY
LOS ANGELES

Department of Electrical and Computer Engineering

EE-2449 Digital Logic Lab

EXPERIMENT 3
LOGIC GATES

Text: Mano and Ciletti, *Digital Design, 5th Edition,* Chapter 2
Required chips:

7400: quad 2-input NAND	**7402**: quad 2-input NOR	**7404**: hex inverters (NOT)
7408: quad 2-input AND	**7432**: quad 2-input OR	**7486**: quad 2-input XOR
7493: 4-bit ripple counter	**7410:** triple 3-input NAND	

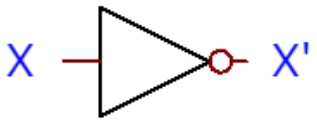
3.1 There are three basic logic functions from which all circuits can be designed: NOT (invert), OR, and AND. In addition, another useful logic function is exclusive-OR or XOR.

The NOT function is also known as INVERT. The NOT function is true (1) if the input is false (0) and vice versa. The logic equation for the inverse of logic variable X is X' (NOT X).

Complete the truth table for the NOT function:

X	X'
0	
1	

The logic gate symbol of a NOT/INVERTER:



It is actually the bubble at the end of the gate that indicates invert. The bubble on the output of any gate means that the output should be inverted.

The AND function is true (1) if both inputs are true (1). The NAND function is an AND-NOT function and is the inverse of an AND function. A NAND function is true (1) if any input is false (0). The logic equation for the AND of two logic variables, X and Y, is X•Y (or XY). The logic equation for the NAND of X and Y is (X•Y)' (or (XY)').

The OR function is true (1) if either input is true (1) or both inputs are true (1). The NOR function is an OR-NOT function and is the inverse of an OR function. A NOR function is true (1) if all inputs are false (0). The logic equation for the OR of two logic variables, X and Y, is X+Y. The logic equation for the NOR of X and Y is (X+Y)'.

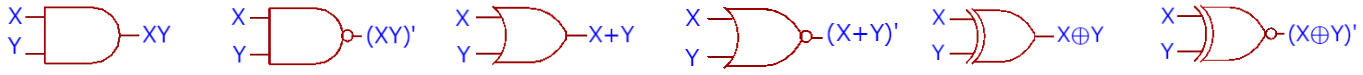
The 2-variable (2-input) XOR function is true (1) if either input is true (1) but not both. The XOR is known as an odd function. If an odd number of inputs are true (1) the output is true (1) – this definition works for any number of inputs. An XNOR is an XOR-NOT function. For a 2-variable (2-input) XNOR function, the function is true (1) if both inputs are the same. The XNOR is known as an even function. If an even number of inputs are true (1) the output is true (1) – this definition works for any number of inputs.

Complete the truth table below for the AND, NAND, OR, NOR, XOR, and XNOR functions.

X	Y	X•Y	(X•Y)'	X+Y	(X+Y)'	X ⊕ Y	(X ⊕ Y)
0	0						
0	1						
1	0						
1	1						

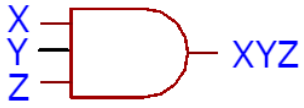
The logic gates for these functions are shown below:

AND NAND OR NOR XOR XNOR

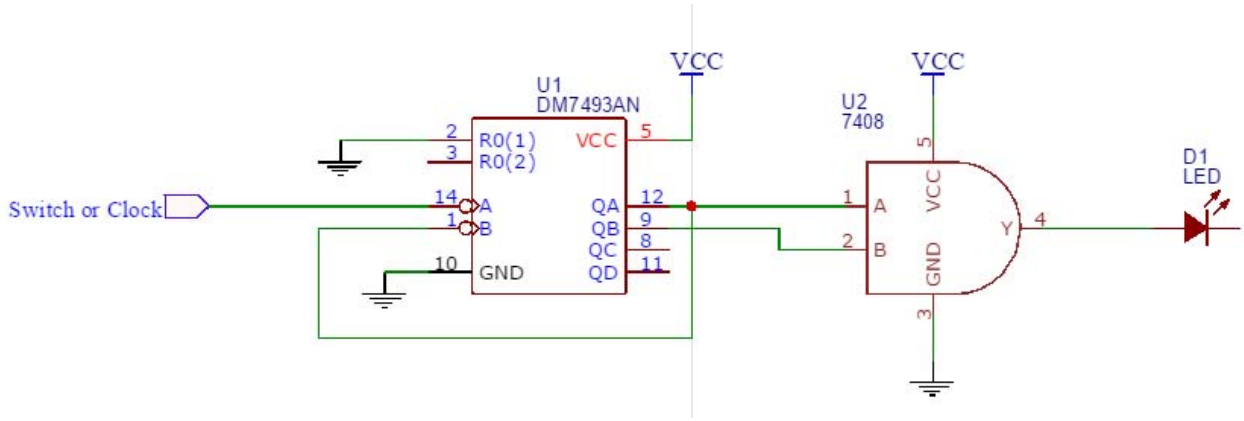


Logic functions can have multiple inputs. Fill in the truth table for the three-input NAND whose gate is shown on the right.

X	Y	Z	(X•Y•Z)'
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

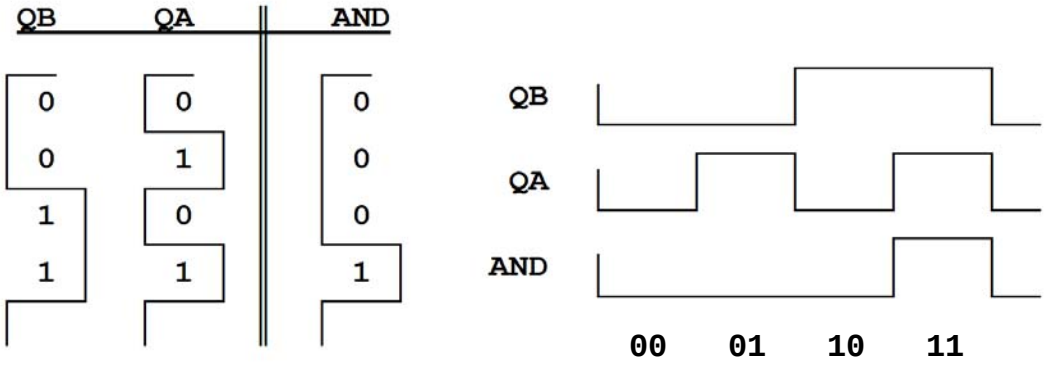


3.2* Set up the 7493 as the binary counter of Experiment 1. (Ground at least one reset input or the chip won't count.) Since counter outputs go through all possible combinations in binary order, they can be used to test the behavior of the various gates listed above.



Connect QB and QA to two inputs of a 7408 AND gate. (Don't forget 5V and ground connections; pins 14 and 7. If you forget, the chip is inactive). Referring to the truth tables in 3.1, Y = QB and X = QA. Connect the clock A input of the counter (pin 14) to the normally high pulser (pushbutton switch). Connect QB, QA, and the output of the AND gate to LEDs and verify that the correct outputs are produced by referring to the truth table below (or your answer to part 3.1).

The truth table and the corresponding waveforms for an AND function are shown below:



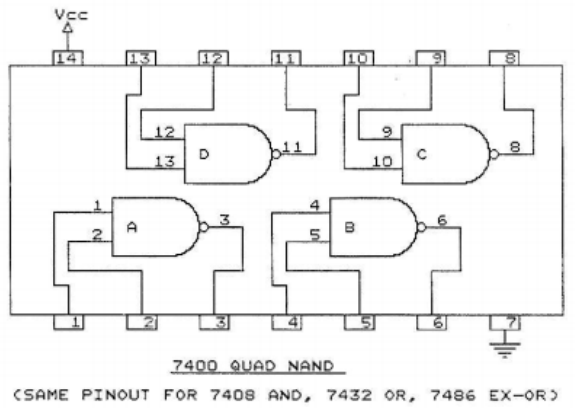
3.3* Notice that the waveforms are just a graphical form of the truth table (rotated 90 degrees counter clockwise). By displaying such waveforms on a scope, you can obtain a description of circuit behavior equivalent to a truth table.

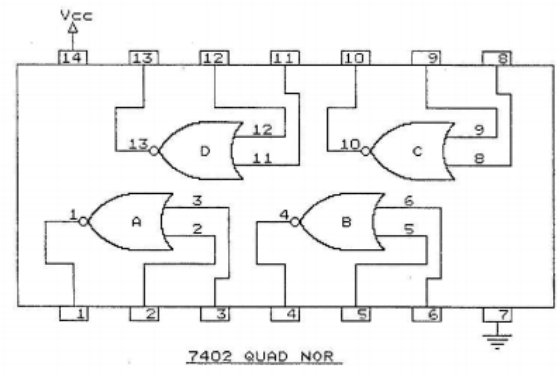
Actually, you don't need both QB and QA on the scope to know where the truth table starts. It always begins where QB, the msb (most significant bit), falls to 0. Thus the true timing relationship of the output to the binary count is seen if just QB and the gate output are shown.

Connect the clock A input (pin 14) to the clock generator. Bring both QB and the AND output to the scope. Adjust the scope's Time/Div until QB goes low for 2 divisions and high for 2 divisions. That way, 4 divisions will represent the full 4-count cycle. Then the AND-gate output should remain low for the first 3 divisions and go high for the 4th only. (Reminder: instructions on using the scope are found at the end of Experiment 2.)

Since a new cycle of 4 counts begins each time QB falls, select negative edge trigger for the channel that displays QB. (Make sure the trigger level lies within QB's waveform.) Draw the waveforms for QB and the AND output in your lab manual. Repeat for a NAND, OR, XOR, and NOR (do the NOR last since it requires some wiring changes). Leave the scope settings alone as you change gates so QB will look the same in all 5 images.

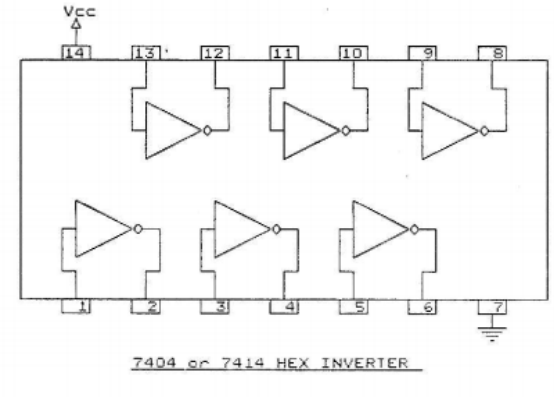
Diagrams for gate chips are found at the very end of this manual and have been provided below for your reference. You will see that those used here have the same power and ground pin numbers (14 and 7). Also, except for the 7402 (NORs), they have exactly the same input and output pin numbers. So, except for the 7402, no wiring changes will be needed as you replace one gate chip with the next. (*Remember to remove chips **gently** so as not to bend pins.)*



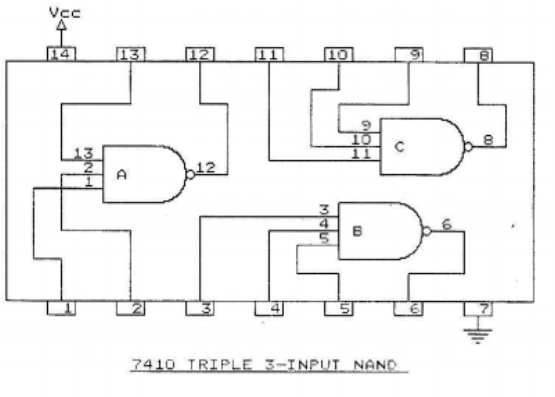


For each logic function, draw the wiring diagram of the logic gate (include the pin numbers) in your lab manual. You do not have to redraw the 7493 counter for each wiring diagram. Just label the inputs of the gates QA and QB. For each logic function draw the waveforms of QB and the output of the respective gate and verify that the output matches your truth table values from section 3.1.

3.4* Also verify the NOT (inverter) function and the 3-input NAND function. Determine how to connect the Q outputs from the counter to drive the logic gates. The diagrams for the hex inverter and 3-input NAND gate chips are shown below (and at the end of the manual). Don't forget to connect power and ground.



7404 or 7414 HEX INVERTER



7410 TRIPLE 3-INPUT NAND

For each logic function, draw the wiring diagram of the logic gate (include the pin numbers) in your lab manual. As before, you do not have to redraw the 7493 counter for each wiring diagram. Just label the inputs of the gates with the appropriate Q output from the counter. For each logic function draw the waveforms of the msb (most significant input bit) and the output of the respective gate and verify that the output matches your truth table values from section 3.1.
